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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/843,630	04/27/2001	Kazuo Nishiyama	09792909-4983	9204

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EXAMINER
MITCHELL, JAMES M

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/843,630	NISHIYAMA, KAZUO	
	Examin r	Art Unit	
	James M. Mitchell	2827	

-- The MAILING DATE of this communication appears on the cover she t with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6 and 7* is/are rejected.

7)☒ Claim(s) *4,8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over General Electric (EP0611129) in combination with Tutsch et al. (U.S 6,630,727).

General Electric (Fig 8a, 8b) henceforth GE discloses (cl. 1) an intermediate semiconductor device fabrication structure comprising: an electronic chip component having all electrodes (15) formed on one surface thereof, side walls thereof being covered with a protective material (24), and wherein there is substantially no protective material located on thee one surface of the chip where all the electrodes are formed (i.e. covered with item 12a) and further wherein the protective material on the side walls wall and a surface of the chip opposite the surface where the electrodes are located have been grinded (810) to a common level and the one surface of the chip where all the electrodes are formed is secured to an adhesive sheet (Col. 2, Lines 45-47) and a plurality of additional same or different electronic chip components also have there respective sides where all the electrodes are formed secured to the adhesive sheet with the protective material located therebetween; (cl. 3) and said semiconductor chip diced at a position of said protective material (i.e. along sidewalls) for mounting on a packaging substrate, wherein all of said side wall is covered with said protective

material (24); (cl. 6) wherein a pseudo wafer (10; i.e. a false semiconductor material with parallel faces used as substrate for IC) comprising a plurality of same or different electronic chip components each having all electrodes form on one surface thereof, which are bonded to each other with a protective material (24) coated on side walls therebetween, and wherein there is no protective material located on the one surface of the chip where all the electrodes (15) are formed and further wherein the protective material on the side wall and a surface of the chip opposite the surface where the electrodes are located have been grinded (810) or polished to a common level and further wherein the plurality of chip components are not originally from a same semiconductor wafer; (cl. 2, 7) and said protective material comprises either one of an organic insulating resin and an inorganic insulating material (i.e. polyimide, epoxy; claim 2 of GE).

GE does not appear to show that the plurality of chips is not originally from a same semiconductor wafer.

Tutsch utilizes chips that are from different semiconductor wafers (i.e. "chips of different types")

It would have been obvious to one of ordinary skill in the art to form the chips of GE from different semiconductor wafers in order to provide a device with memory and processor as taught by Tutsch (Col. 4, Lines 60-63).

Furthermore it would have been obvious to form the chips from different wafers for cost efficiency as admitted by applicant (Specification Page 11).

Response to Arguments

Applicant's arguments with respect to amendment have been considered but are moot in view of the new ground(s) of rejection.

However, applicant's argument that "only those chips that are not defective are further processed is moot, because that limitation is not claimed.

Allowable Subject Matter

Claims 4, 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art does not disclose or make obvious forming solder bump on each of said electrodes including all the limitations of the independent claims or dicing said psuedo wafer into a single semiconductor chip at a position of said protective material for mounting on a packaging substrate including all the limitations of the independent claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 10:30-8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jmm
July 6, 2004

KAMAND CUNEO
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